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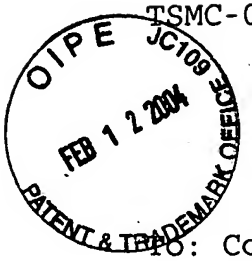


February 5, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/083,991 02/26/02 |

Chia-Der Chang et al.

PLANARIZATION METHOD FOR DEEP SUB MICRON SHALLOW TRENCH ISOLATION PROCESS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 9, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date _____ 2/9/04

This Information Disclosure Statement is being filed after the mailing date of a Final Action under 1.113 or a Notice of Allowance under 1.311, whichever comes first, but before, or simultaneously with, the payment of the Issue Fee.

The Commissioner is authorized to charge the IDS processing fee of $180 under 37 CFR 1.17(p) to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

TW Publication No. 299463/406359/364166 discusses a method for forming a gap-filled, planarization structure of dielectric materials on a substrate topography useful for forming micro-electronic devices.

Sincerely,

George O. Saile

George O. Saile,
Reg. No. 19,572

Form PTO-1449

# INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE JC109 FEB 12 2004 PATENT & TRADEMARK OFFICE

| Docket Number (Optional) | Application Number |
|---|---|
| TSMC-01-660 | 10/083,991 |
| Applicant: Chia-Der Chang et al. | |
| Filing Date: 02/26/02 | Group Art Unit |

## U. S. PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
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## FOREIGN PATENT DOCUMENTS

| | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation YES | Translation NO |
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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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| | TW Publication No. 299463/406359/364166. |
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| EXAMINER | DATE CONSIDERED |
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

IW. publication No.
599463

A method for forming a gap-filled, planarization structure of dielectric materials on a substrate topography useful for forming microelectronic devices. A dielectric material is first deposited as continuous, dry dielectric layer, preferably a SOG layer. Then the dielectric layer is partially removed by chemical-mechanical-polishing (CMP). The chemical and mechanical properties of the structure can be chosen by varying the composition of the SOG layer and the subsequent CMP conditions.

TW publication No.
406359

1.A method of Chemical Mechanical Polishing (CMP) a low-k spin-on glass (SOG) oxide layer of a semiconductor device, comprising:

(a) providing a substrate with bumpy topography;

(b) forming a low-k SOG oxide layer on said substrate;

(c) planarizing said low-k SOG oxide layer by using a $CeO_2$-based slurry which contains tetra-alkyl substitute ammonium hydroxide surfactant.

TW Publication No.
364166

Structure and process for a multi-layer spin-on material are used. Process duration of a semiconductor planarization process is easy to control and manage by Chemical Mechanical Polishing (CMP) with this material. Two kinds of spin-on materials with different removal rates are used. The material with lower removal rate (a buffer layer) is formed on a semiconductor substrate first, and then the other material with higher removal rate is formed on the top. Afterwards, the polishing thickness can be controlled with the buffer layer when polished near the semiconductor substrate.